

Online Reprogrammable Multi Tenant Switches

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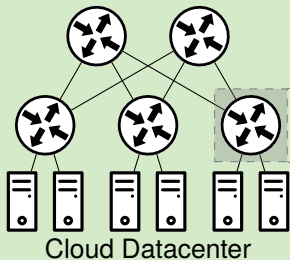
- On switch ...
 - ▶ ...stateful load balancer **replaces hundreds of servers** [SilkRoad 2017]
 - ▶ ...data aggregation **speeds up databases** [Lerner et.al. 2019, ...]
 - ▶ ...paxos **reduces coordination overhead** [NetChain 2018, ...]
 - ▶ ...key-value caching **improves throughput and latency** [NetCache 2017, ...]

Programmable Switch as a Service

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Programmable Switch as a Service



Tenant 1:
Load Balancer

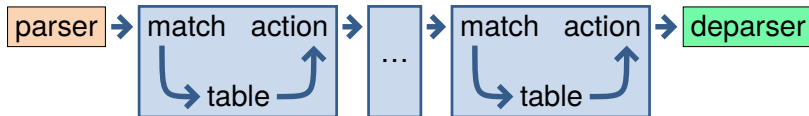
Tenant 2:
SQL group-by

Tenant 3:
PAXOS node

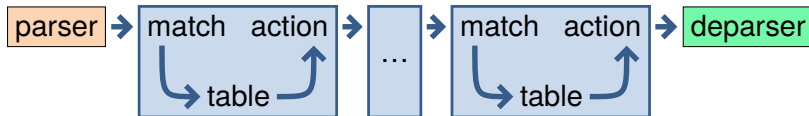
Tenant 4:
Key-Value Cache

Packet Forwarding

Current Programmable Switch Pipeline [RMT 2013, Barefoot Tofino]

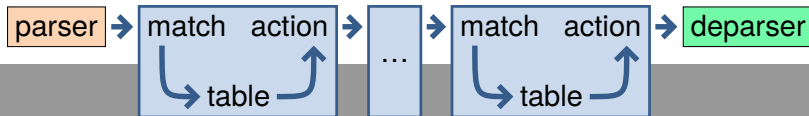


Current Programmable Switch Pipeline [RMT 2013, Barefoot Tofino]



- Runs a single P4 program

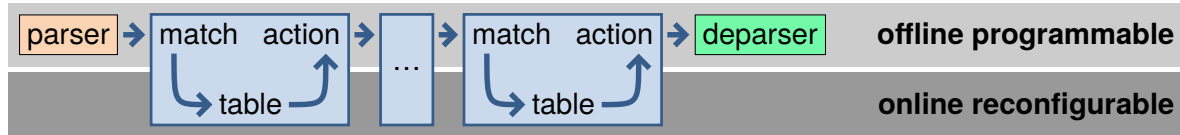
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online reconfigurable

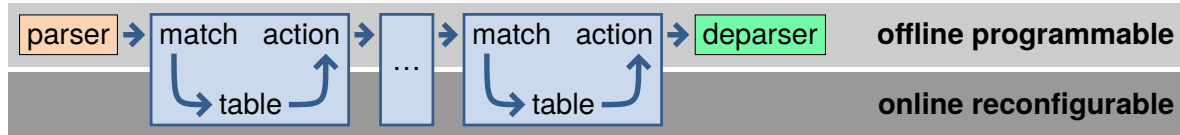
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- Runs a single P4 program
- Reprogramming causes switch and network **downtime**

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We propose to modify the programmable switch architecture

- To enable hot-pluggability of on-switch functions

Definition

The ability to **insert**, **modify**, and **remove** on-switch functions **without affecting** other on-switch functions and packet forwarding.

Tenant 1:

Load Balancer

needs high availability

Tenant 2:

SQL group-by

lifetime of seconds

Packet Forwarding

Programmable Switch

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Related Work

- **Use a dedicated switch for each application** [PPS 2019]
- **Put generalized functionality permanently onto switches** [NetAccel 2019, Ports et al. 2019]
- **Emulate P4 in Match-Action Tables** [Hyper4 2016, HyperVDP 2019]
 - ▶ Excessive Resource Consumption

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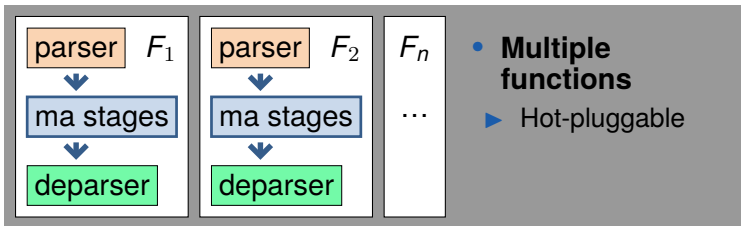
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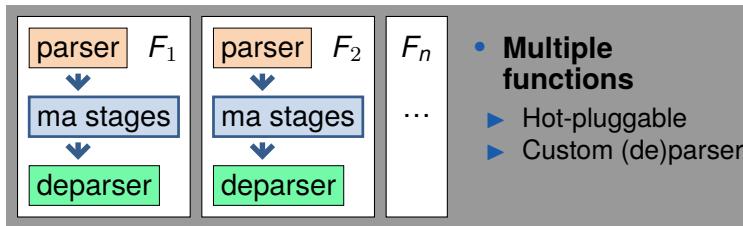
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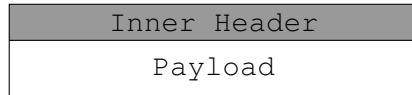
We want: **Switch Sharing & On-Demand Instantiation & Individual Customization**

Switch Architecture Requirements

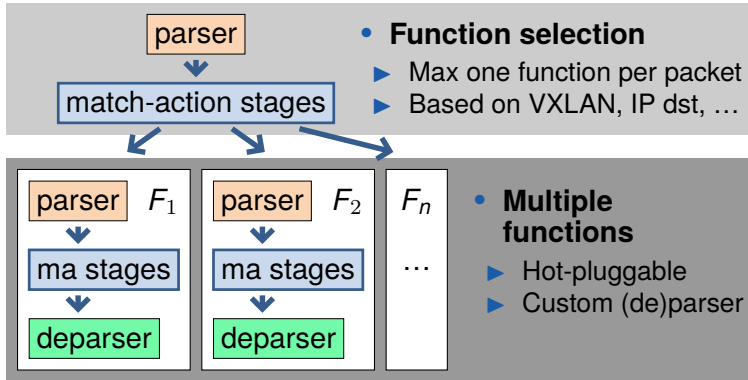




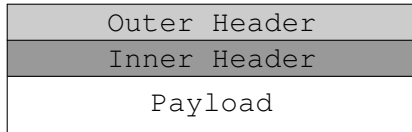
Packet Structure



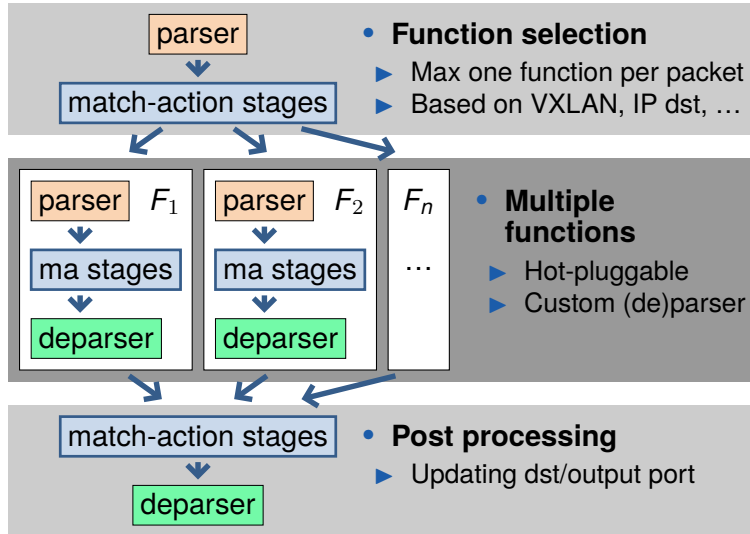
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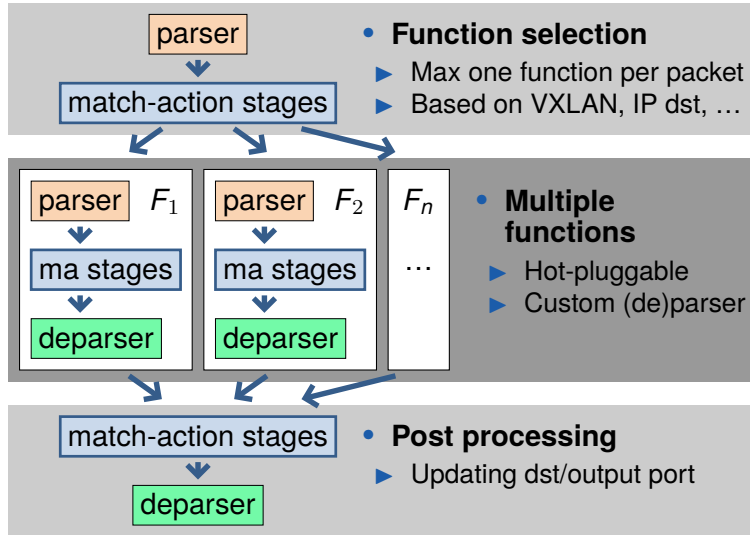
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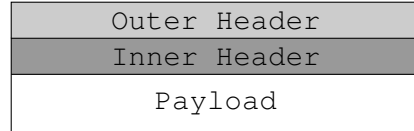
Packet Structure

Outer Header
Inner Header
Payload

Switch Architecture Requirements



Packet Structure



Program isolation

- Access to only own packets
- Limit access to outer header
- Control plane virtualization

- We present three different possible implementations
 - ▶ None of them yet implemented

Multiple Switching ASICs

- ✓ Easily realizable
- ✗ No statefull functions

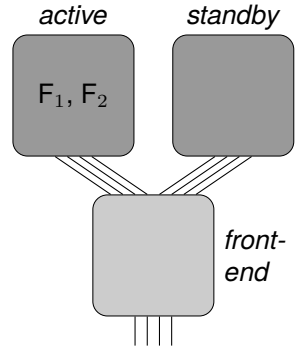
Using FPGAs

- ✓ Realizable with FPGA knowledge
- ✗ Reduced Throughput

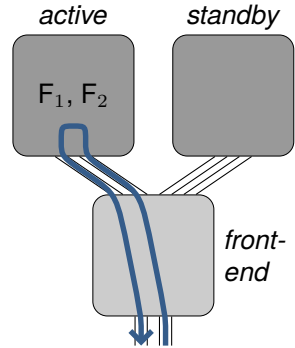
An ASIC extension

- ✗ To be done by switching ASIC vendors
- ✓ High performance

- Alternate between two switching ASICs

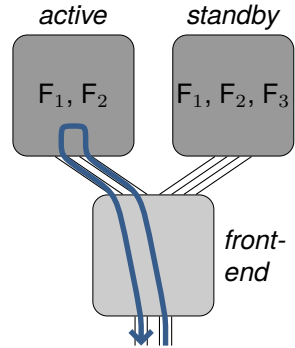


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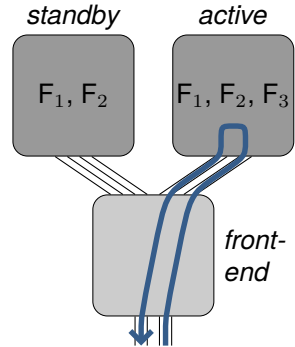
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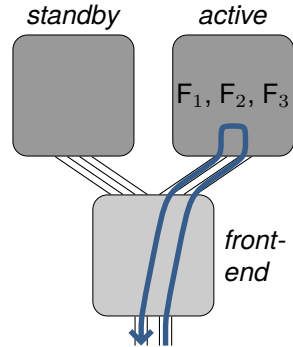


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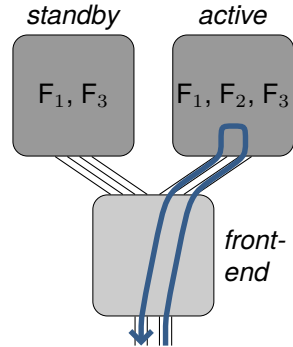
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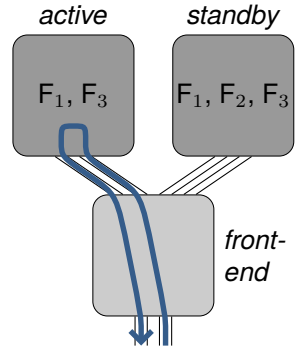


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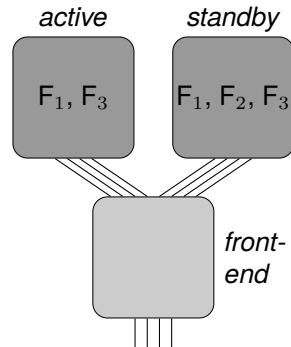
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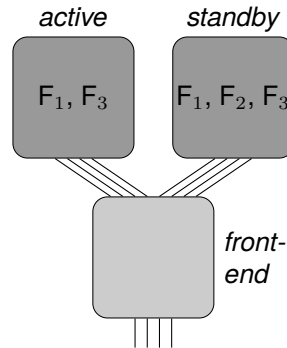
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- Merge functions into single program



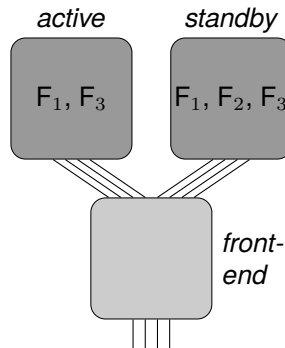
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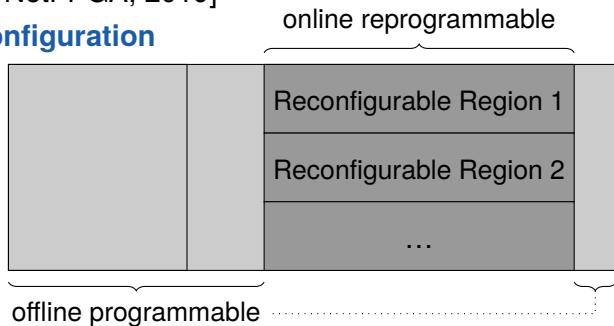
- ✓ Based on available hardware

Limitations

- ✗ Problematic for statefull functions

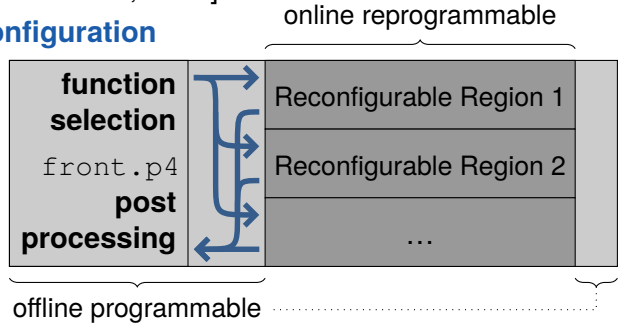
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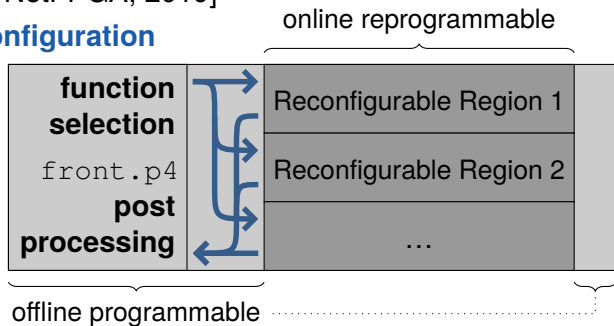


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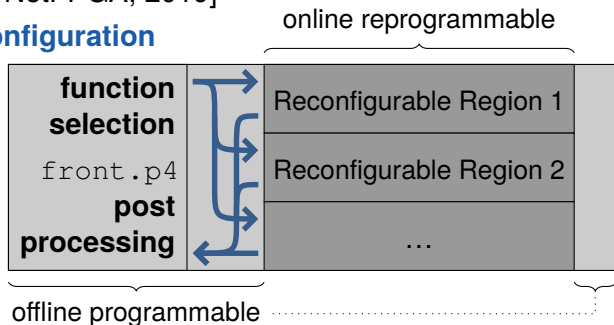
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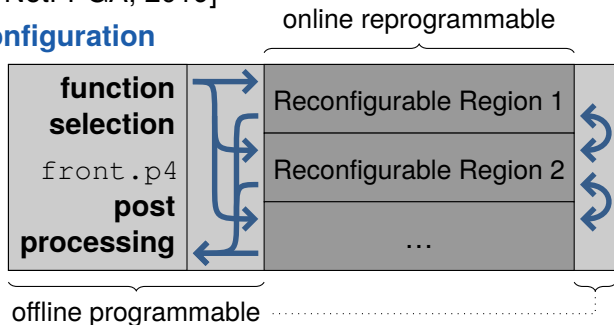
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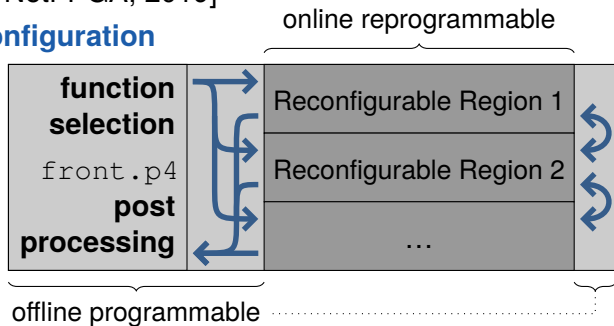


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Advantages

- ✓ Readily available hardware
- ✓ Non-reconfigured regions keep state

Limitations

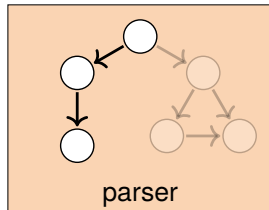
- ✗ Limited throughput

An extension to current switching ASICs

- **Parser, matching, actions, and deparser are stored in SRAM and TCAM**
 - ▶ Use per entry validity bit for atomic updating [CoPTUA 2004]

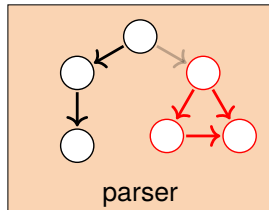
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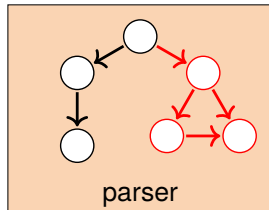
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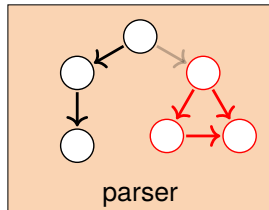
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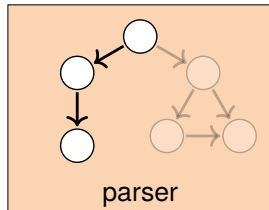
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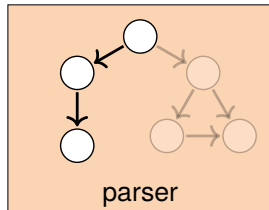
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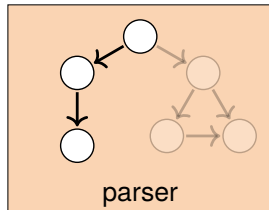
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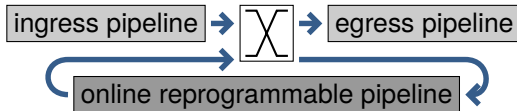
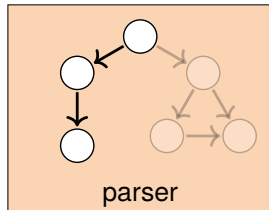
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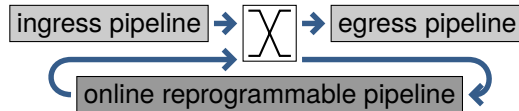
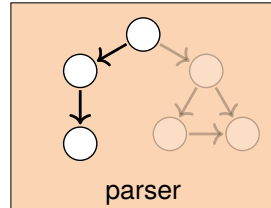
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Limitations

- ✗ Needs to be done by ASIC vendors

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- **We propose an architecture for online reprogrammability**
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New interesting resource management questions

- Measuring & accounting resource usage
- Resource allocation
- Avoiding resource fragmentation
- ...