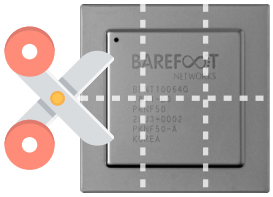

Slicing Match-Action Pipeline Resources for Multitenancy on Programmable Switches

Johannes Krude, Felix Frei, Pedram Ahmadiyeh,
René Glebke, Mirko Stoffers, Klaus Wehrle

RWTH Aachen University

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DFG Collaborative Research Centre 1053 – MAKI
Multi Mechanism Adaptation for the Future Internet

NetSoft, 2025-06-26

COM SYS | RWTH AACHEN UNIVERSITY

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Implemented for Tofino

- **Eval on real P4 programs**
- **Sourcecode on GitHub**

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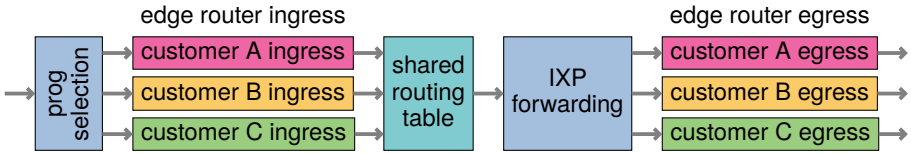

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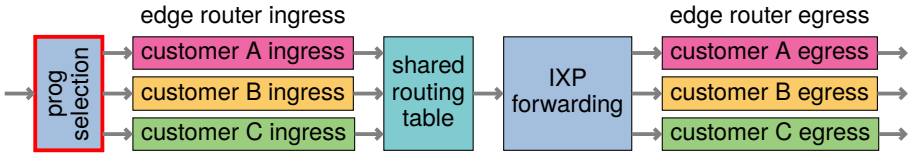

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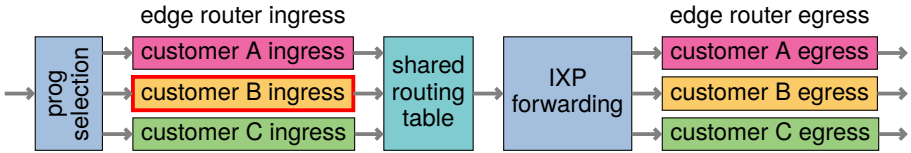

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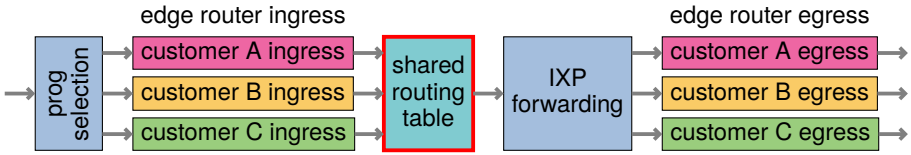

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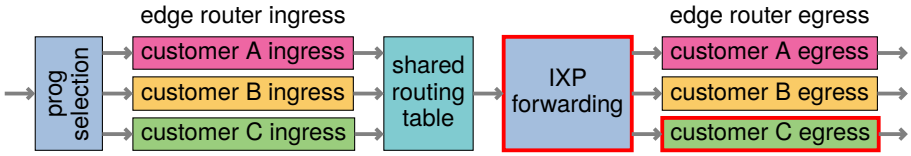

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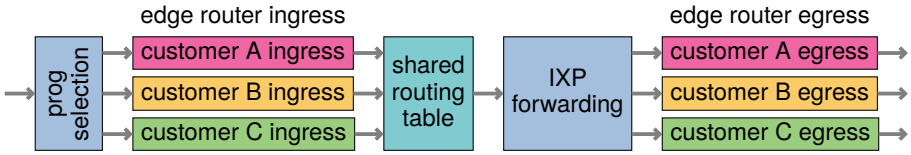

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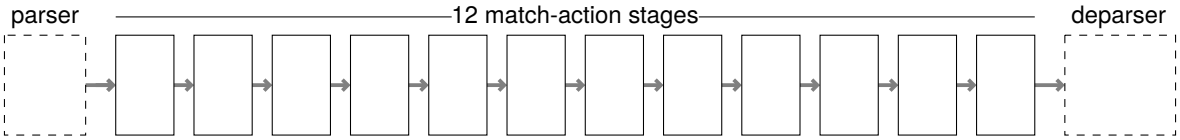
Requirements for switch sharing

- **Safely composing programs** [P4Weaver, Wang et.al. 2020, P4Visor, P4Brick]
- **(Our Contribution): Guaranteed switch pipeline resources for each customer**

Pipeline Resources



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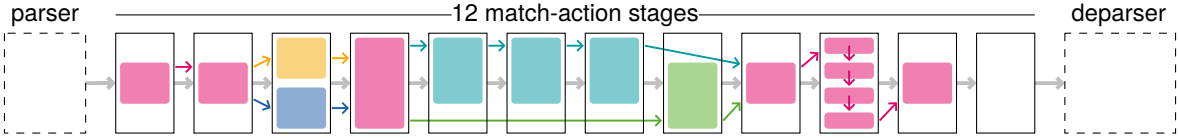
Pipeline Resources



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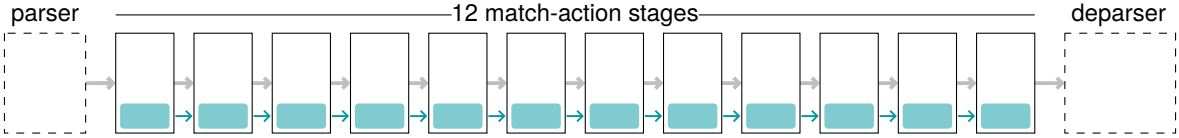

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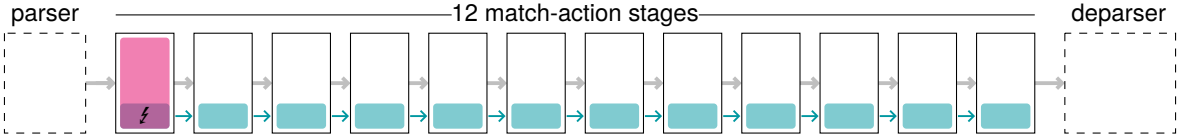

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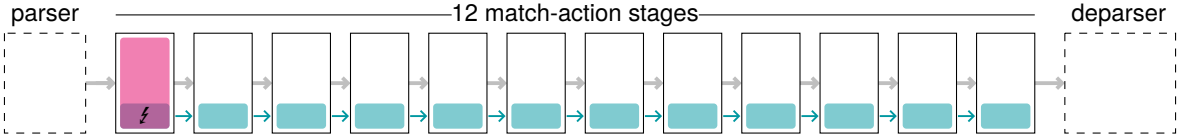

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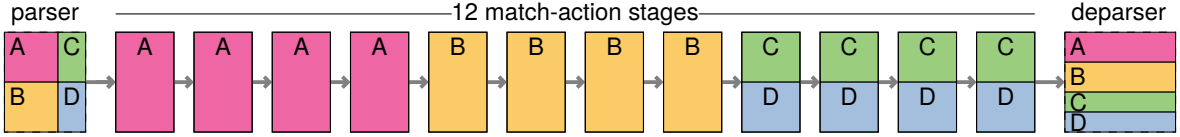
Tenants should know in advance the acceptable resource usage and program shape

Slicing Match-Action Pipeline Resources



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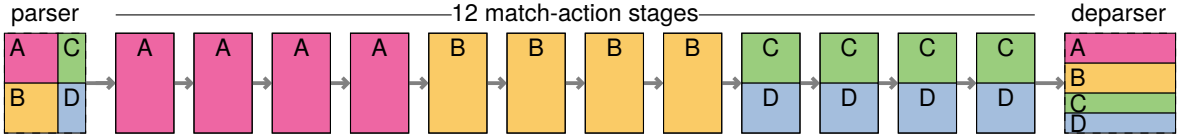

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divides pipeline into slices

negotiate pipeline slice

Tenant

creates or adapts program

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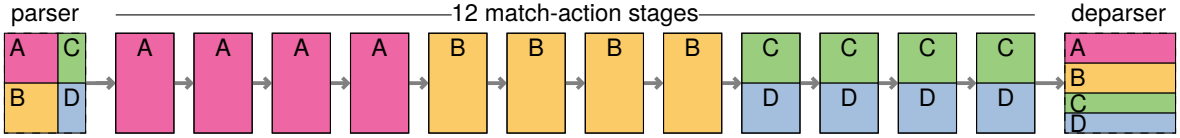

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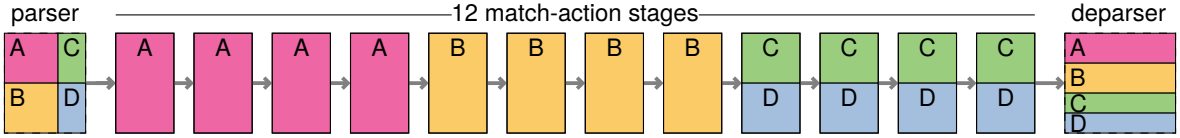

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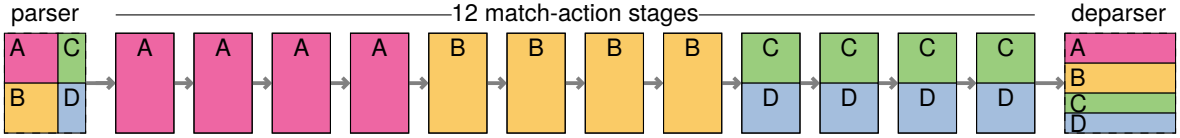

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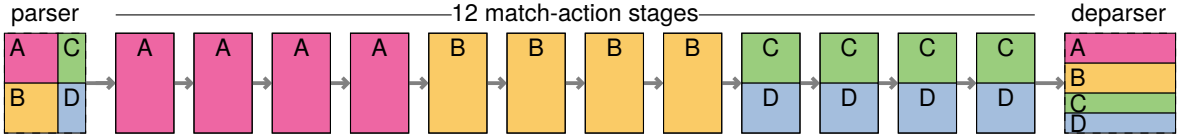

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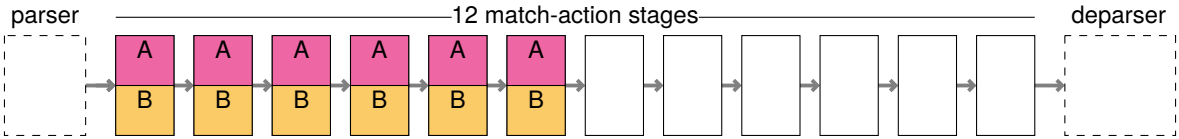
Slice checking guarantees all other tenants the availability of resources

Program and Slice Shapes

Slices are only useful if the tenant program can be shaped to fit into the slice

Same slice for each tenant → Little flexibility

Individual slice shapes → Unallocated leftover resources



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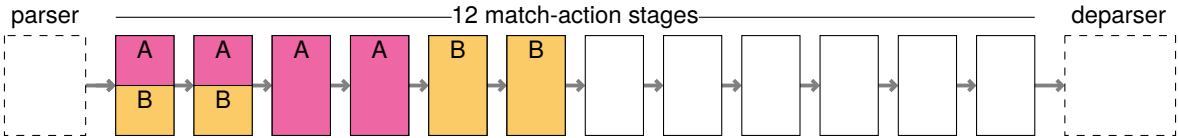

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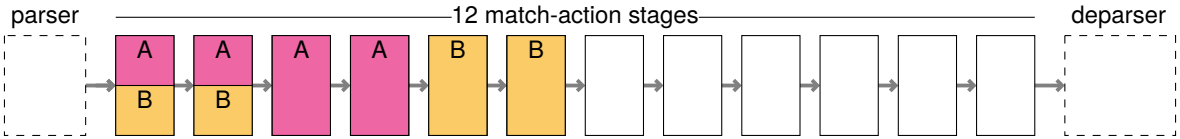

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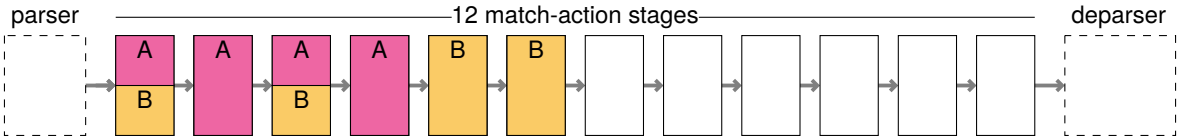

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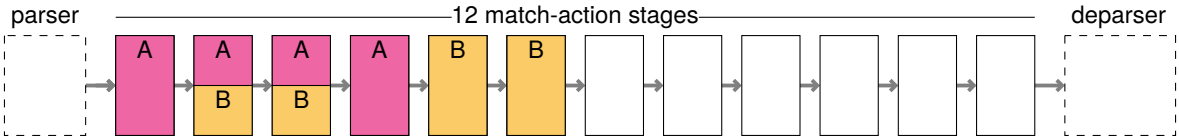

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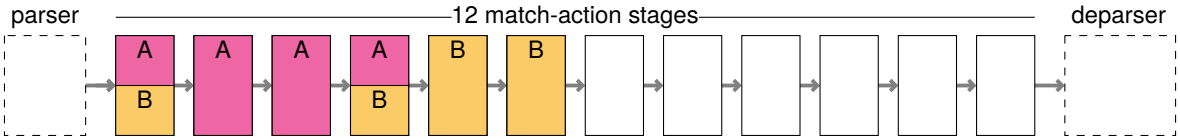

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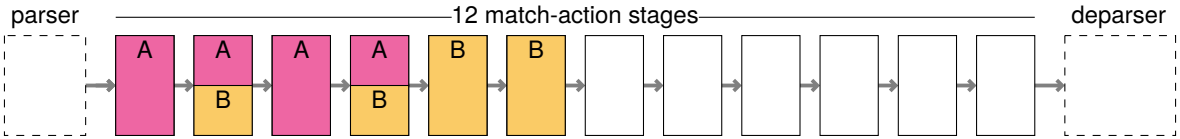

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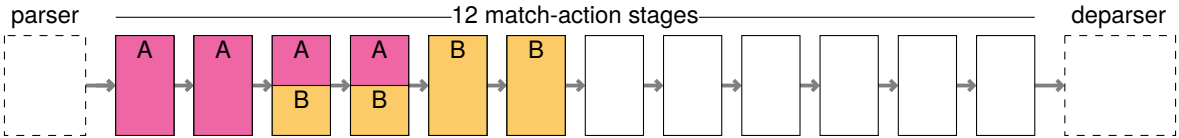

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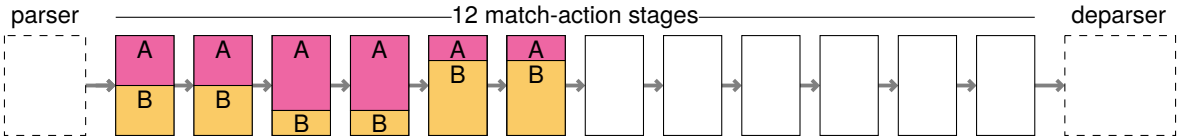

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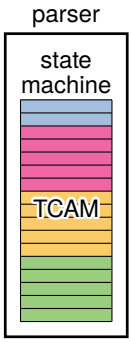

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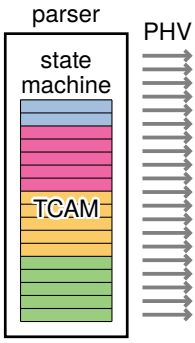
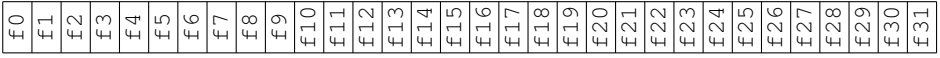


packet header vector (PHV)



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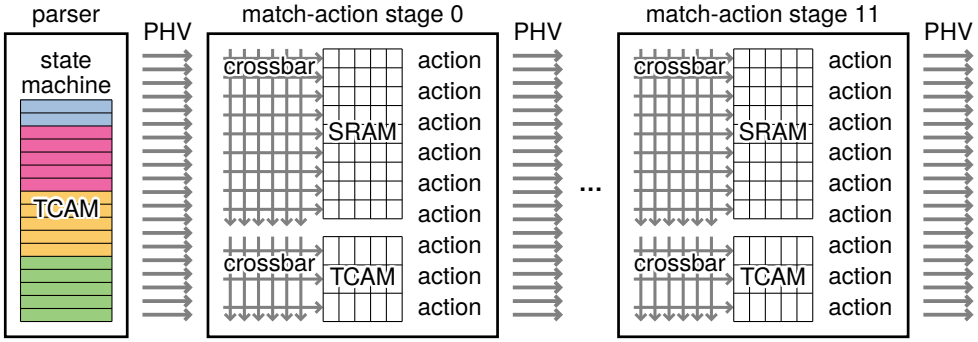

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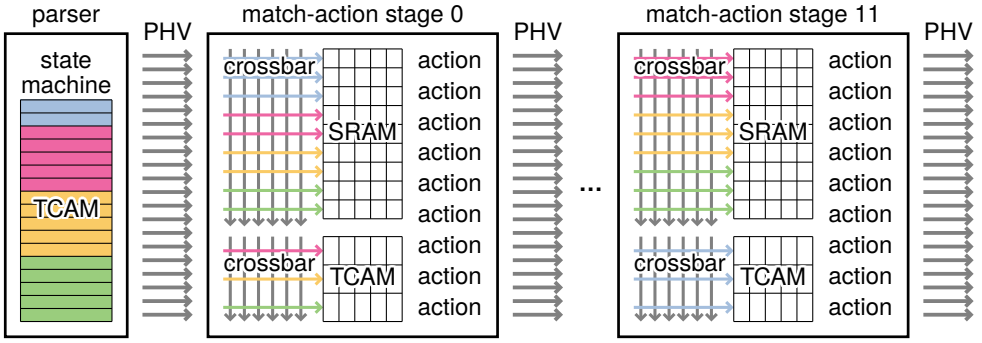

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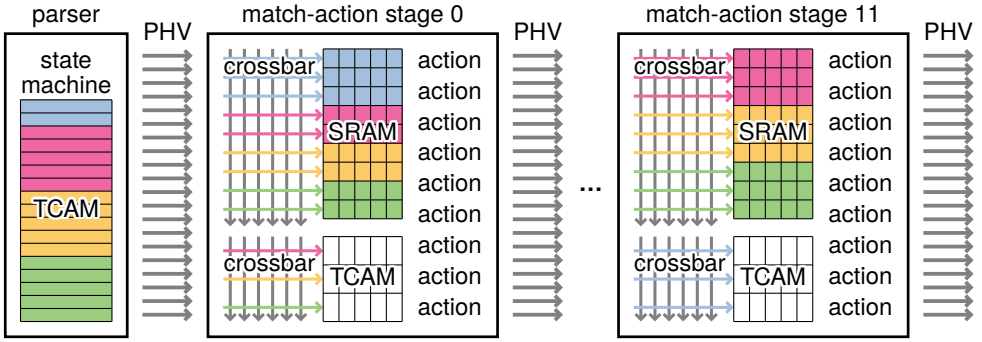

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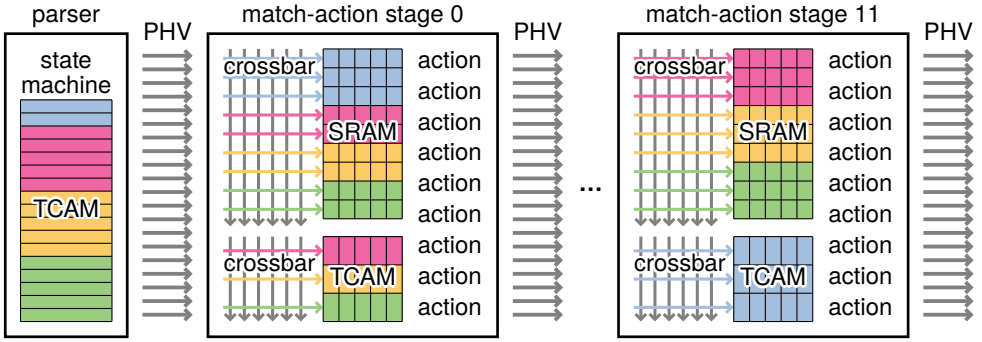

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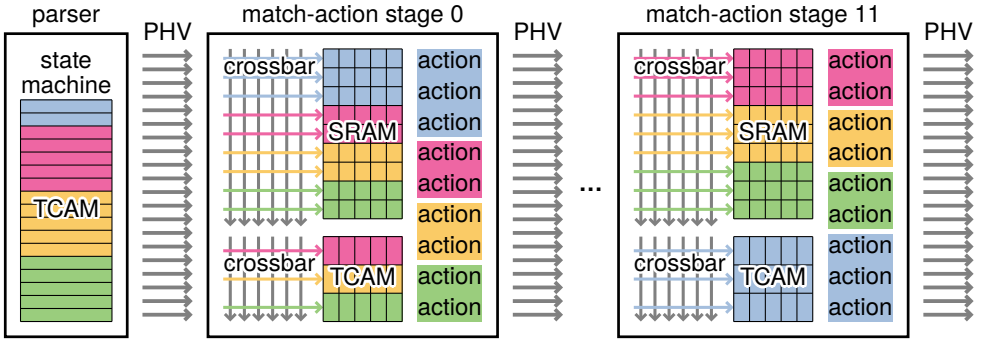

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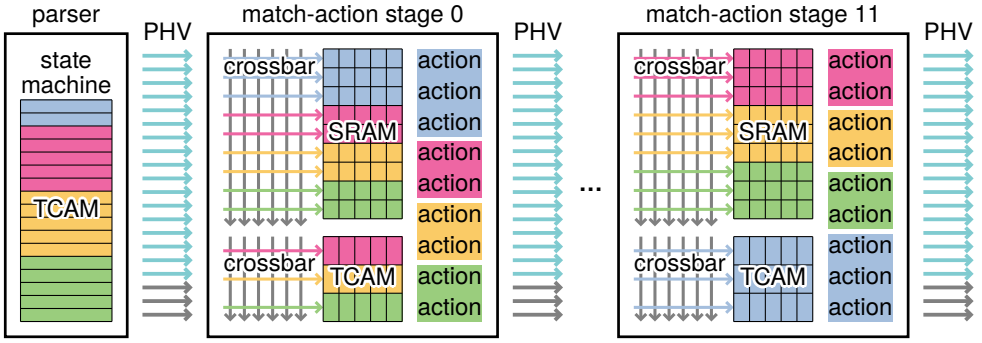

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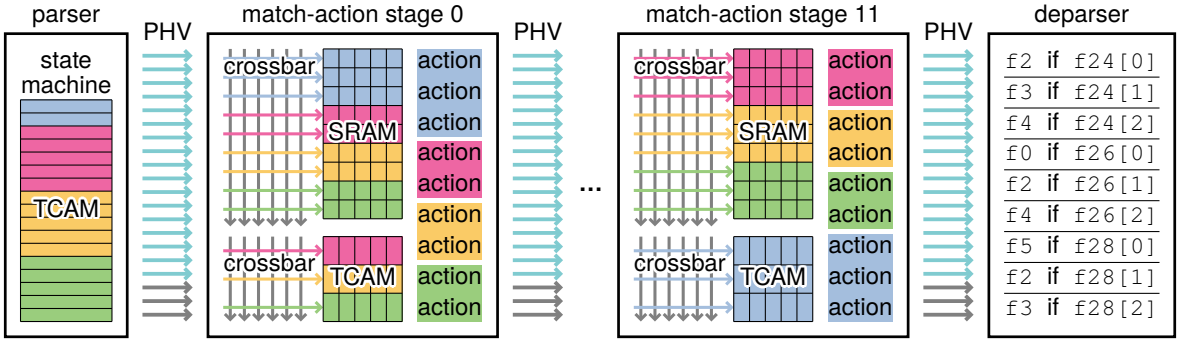

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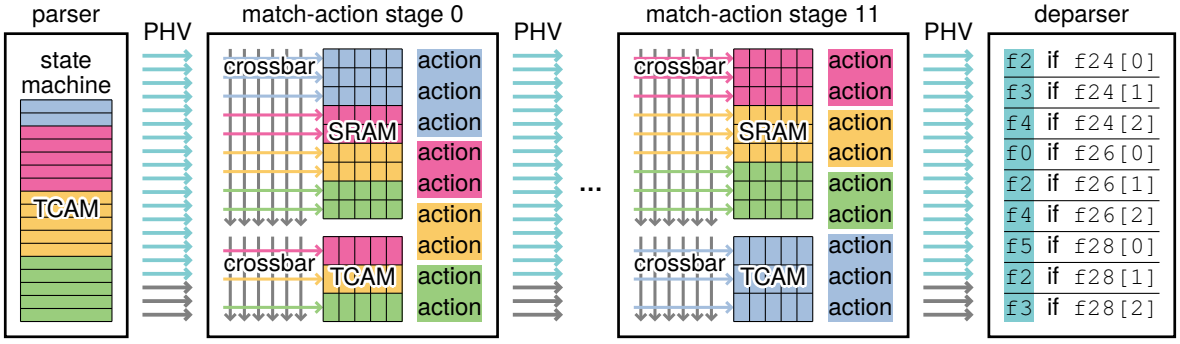

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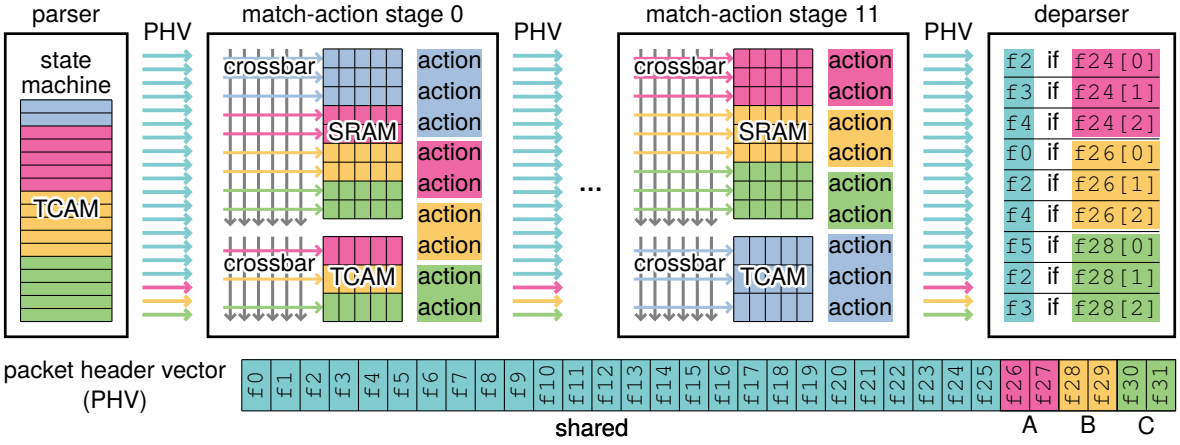

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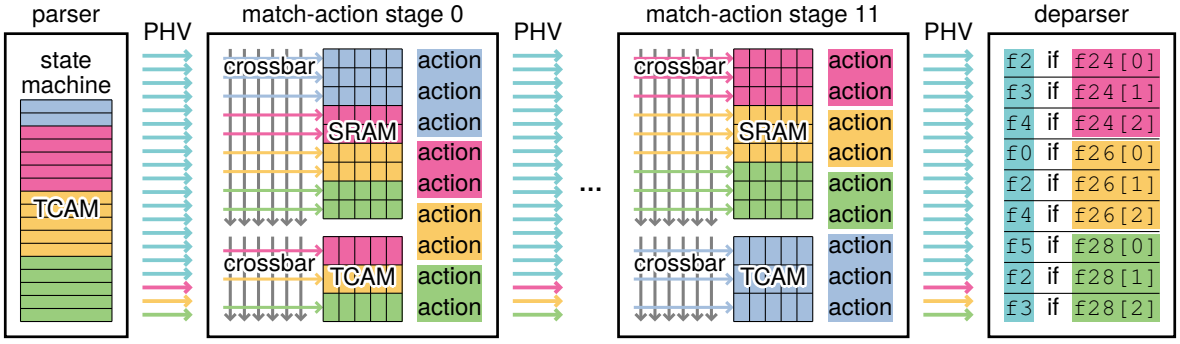

Most of the packet header vector can be shared, except for the validity bits

Slicing Tofino

- **Each pipeline has 16x 100 GbE port → target up to 16 slices per pipeline**

Parser
- Up to 256 slices

Deparser
- Up to 192 slices

Packet header vector
- Up to 48 slices, each with 16+16 validity bits and 128 shared fields

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Match Action Stages
- Crossbars only dividable into three identical slices

Stage Division	$1/1$
	$1/2$
	$1/3$

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		Stages per Slice					
		12	6	4	3	2	1
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		Stages per Slice						
		12	6	4	3	2	1	
Stage Division	$^1/_1$	1	2	3	4	6	12	*Number of Slices*
	$^1/_2$	2	4	6	8	12	24	
	$^1/_3$	3	6	9	12	18	36	

- Up to 36 identical slices

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Stage Division	$1/1$	1	2	3	4	6	12	*Number of Slices*
	$1/2$	2	4	6	8	12	24	
	$1/3$	3	6	9	12	18	36	

- Up to 36 identical slices

Implemented slice checking and program composition on Barefoot Assembly (.bfa) files

Compiling P4 for a Slice

Implemented 3 variants

1. **Modified bf-p4c**
   - No PHV constraints
2. **SMT table placement**
   - Reordering stages
3. **Add additional tables**
   - Unmodified compiler

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Compiled 19 P4 programs from various sources

Program	Smallest Slice
RTT	$12 \cdot 1/1$
firewall	$6 \cdot 1/1$, $12 \cdot 1/2$
chord	$4 \cdot 1/1$, $12 \cdot 1/3$
accelerator	$4 \cdot 1/2$
source_routing	$4 \cdot 1/3$
flowlet	$2 \cdot 1/2$
qos	$2 \cdot 1/3$
ecn	$2 \cdot 1/3$
MPLS	$1 \cdot 1/2$

Program	Smallest Slice
IXP_routing	$4 \cdot 1/1$
aes	$12 \cdot 1/3$
conquest_b.	$2 \cdot 1/1$, $4 \cdot 1/2$
speedtest	$2 \cdot 1/1$, $4 \cdot 1/2$, $6 \cdot 1/3$
a._tunnel	$2 \cdot 1/2$
firewall_s.	$1 \cdot 1/1$, $2 \cdot 1/2$, $3 \cdot 1/3$
calc	$1 \cdot 1/2$
single_table	$1 \cdot 1/3$
VXLAN	$3 \cdot 1/2$
multicast	$1 \cdot 1/2$

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Program	Prog. Instances **Slicing**
RTT	1
firewall	2
chord	3
accelerator	6
source_routing	9
flowlet	12
qos	18
ecn	18
MPLS	24

Program	Prog. Instances **Slicing**
IXP_routing	3
aes	3
conquest_b.	6
speedtest	6
a._tunnel	12
firewall_s.	12
calc	24
single_table	36
VXLAN	**8**
multicast	**24**

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X. Merge P4 programs
- Similar to related work
- Compile merged P4

Compiled 19 P4 programs from various sources

Program	Prog. Instances **Slicing**	Merge
RTT	1	
firewall	2	
chord	3	
accelerator	6	
source_routing	9	
flowlet	12	
qos	18	
ecn	18	
MPLS	24	

Program	Prog. Instances **Slicing**
IXP_routing	3
aes	3
conquest_b.	6
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Program	Prog. Instances **Slicing**		Merge
RTT	1	<	2
firewall	2	<	4
chord	3	<	7
accelerator	6	<	9
source_routing	9		
flowlet	12		
qos	18		
ecn	18		
MPLS	24		

Program	Prog. Instances **Slicing**
IXP_routing	3
aes	3
conquest_b.	6
speedtest	6
a._tunnel	12
firewall_s.	12
calc	24
single_table	36
VXLAN	**8**
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Program	Prog. Instances **Slicing**		Merge
RTT	1	$<$	2
firewall	2	$<$	4
chord	3	$<$	7
accelerator	6	$<$	9
source_routing	9	$\approx$	10
flowlet	12	$\approx$	13
qos	18	$\approx$	21
ecn	18	$\approx$	21
MPLS	24	$\approx$	32

Program	Prog. Instances **Slicing**	Merge
IXP_routing	3	
aes	3	
conquest_b.	6	
speedtest	6	
a._tunnel	12	
firewall_s.	12	
calc	24	
single_table	36	
VXLAN	**8**	
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accelerator	6	$<$	9
source_routing	9	$\approx$	10
flowlet	12	$\approx$	13
qos	18	$\approx$	21
ecn	18	$\approx$	21
MPLS	24	$\approx$	32

Program	Prog. Instances Slicing		Merge
IXP_routing	3	$=$	3
aes	3	$=$	3
conquest_b.	6	$=$	6
speedtest	6	$=$	6
a._tunnel	12	$=$	12
firewall_s.	12	$=$	12
calc	24	$=$	24
single_table	36	$=$	36
VXLAN	**8**		
multicast	**24**		

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RTT	1	$<$	2
firewall	2	$<$	4
chord	3	$<$	7
accelerator	6	$<$	9
source_routing	9	$\approx$	10
flowlet	12	$\approx$	13
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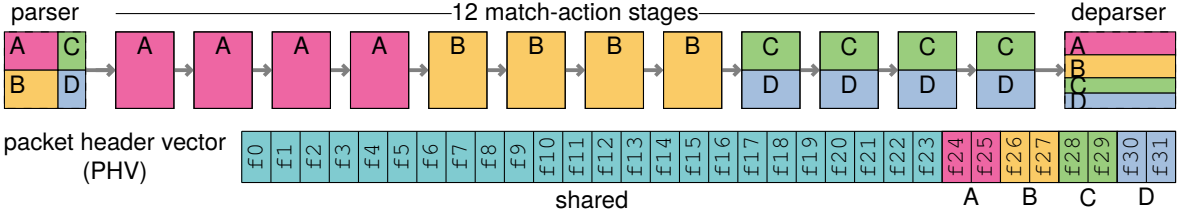
ecn	18	$\approx$	21
MPLS	24	$\approx$	32

Program	Prog. Instances Slicing		Merge
IXP_routing	3	$=$	3
aes	3	$=$	3
conquest_b.	6	$=$	6
speedtest	6	$=$	6
a._tunnel	12	$=$	12
firewall_s.	12	$=$	12
calc	24	$=$	24
single_table	36	$=$	36
VXLAN	**8**	$>$	6
multicast	**24**	$>$	15

Conclusion

- **Resource guarantees for multitenany on match-action pipelines**
  - ▶ Provider divides pipeline into slices
  - ▶ Provider checks program for slice
  - ▶ Tenant compiles program for slice
- **Our packet header vector sharing approach can increase switch utilization**



Full implementation, all example programs, and scripted eval on GitHub